

The diagram illustrates a multi-processor system architecture. On the left, a vertical bar represents the **MP/MCD SYSTEM**. Four **PROCESSOR** units are connected to this system. Each processor contains a **CACHE** and an **OS** (with **DOS** as a sub-component). Each processor is connected to an **ADAPTER** via a bidirectional arrow. The adapters are connected to an **INTER-PROCESSOR BUS**, which is represented by a central vertical line with horizontal connections to each adapter. Above the bus, there are four control blocks: **BINDING**, **BINDING MAPPER**, **ADDRESS MAPPER** (containing an **ADDRESS MAP**), and **A/DDC PROGRAMS**. Bidirectional arrows connect these blocks in a vertical stack. The **INTER-PROCESSOR BUS** also has bidirectional connections to each **ADAPTER** and to the **ADDRESS MAPPER**. To the right of the bus, a **SWITCH** connects the adapters to a vertical column of **AP** (Application Processor) blocks. Each **AP** block is connected to a **DP** (Data Processor) block, which in turn is connected to a **DISK DRIVE**. The **ADDRESS MAPPER** also has a bidirectional connection to the **A/DDC PROGRAMS** block.

FIG. 1  
PRIOR ART

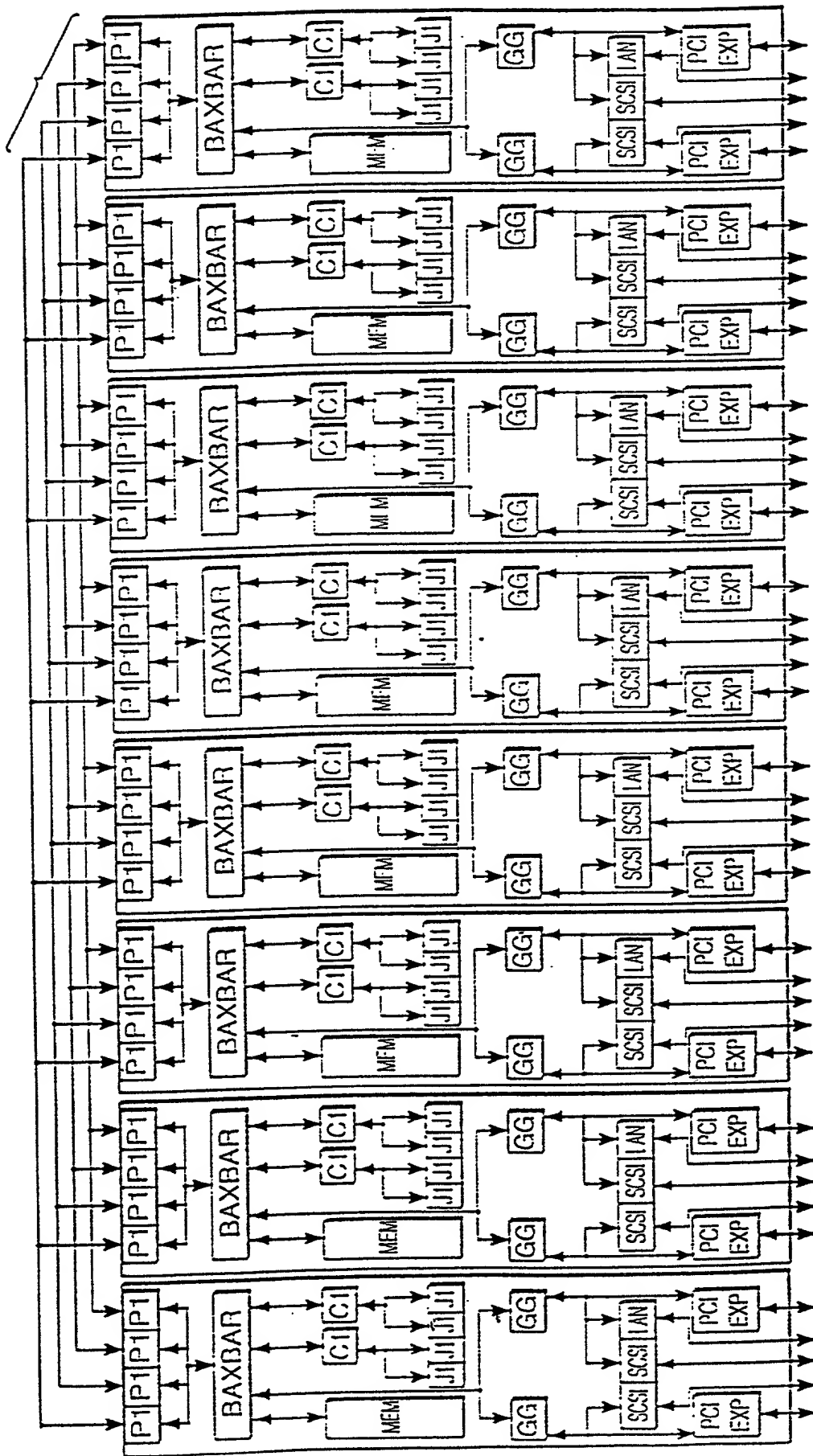


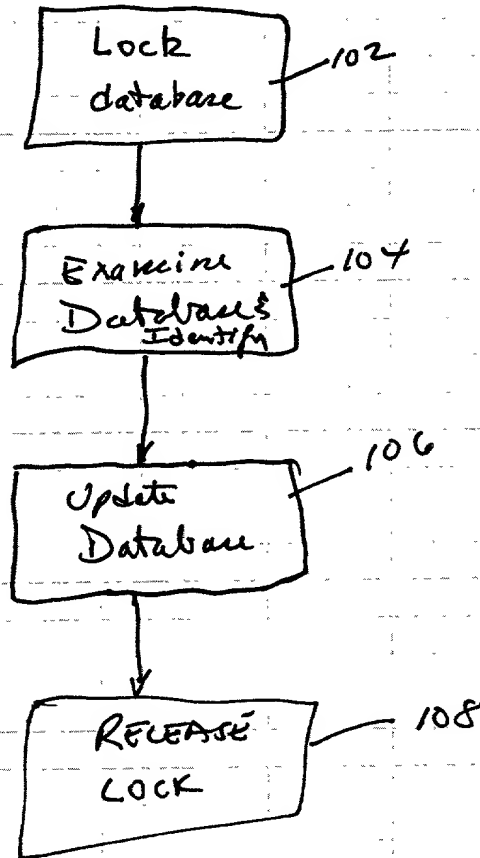
FIG. 2  
PRIOR ART

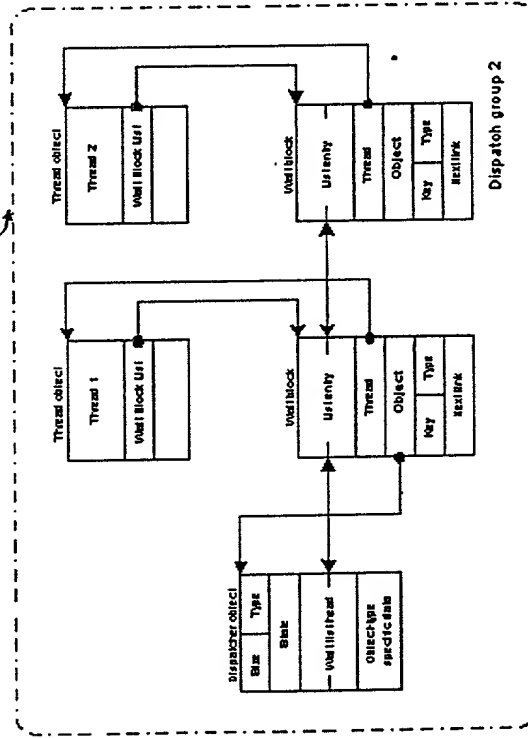
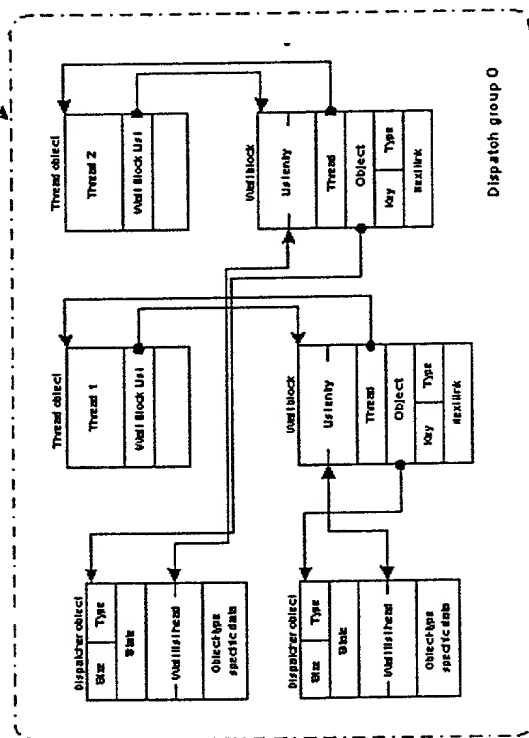
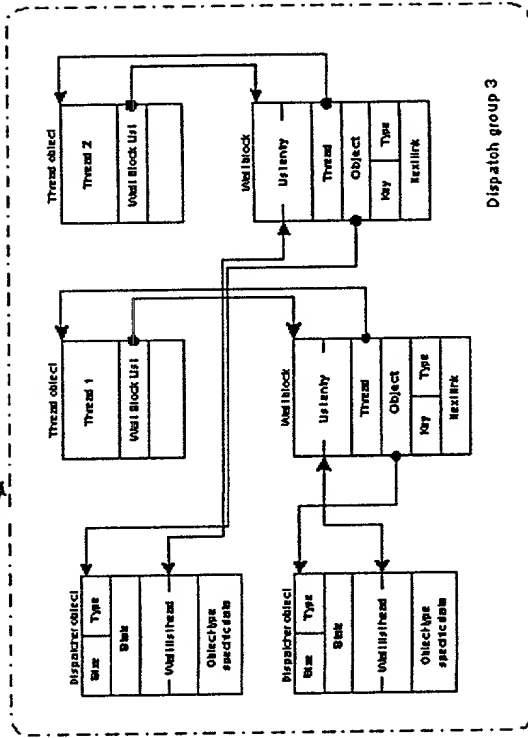
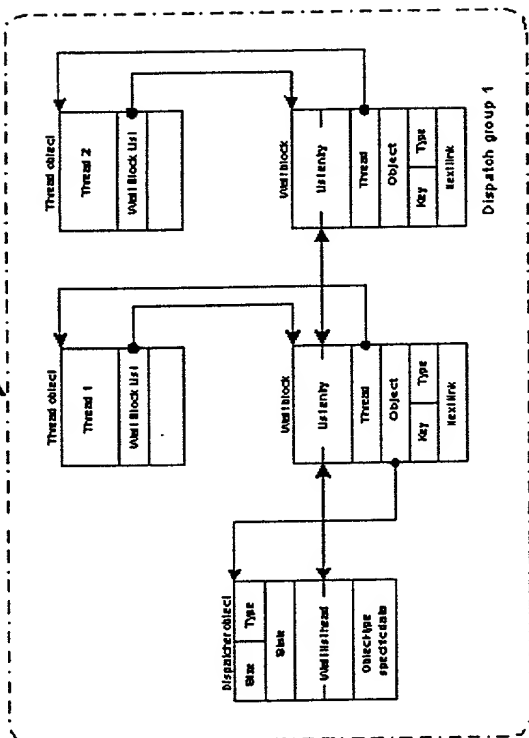






FIG. 5





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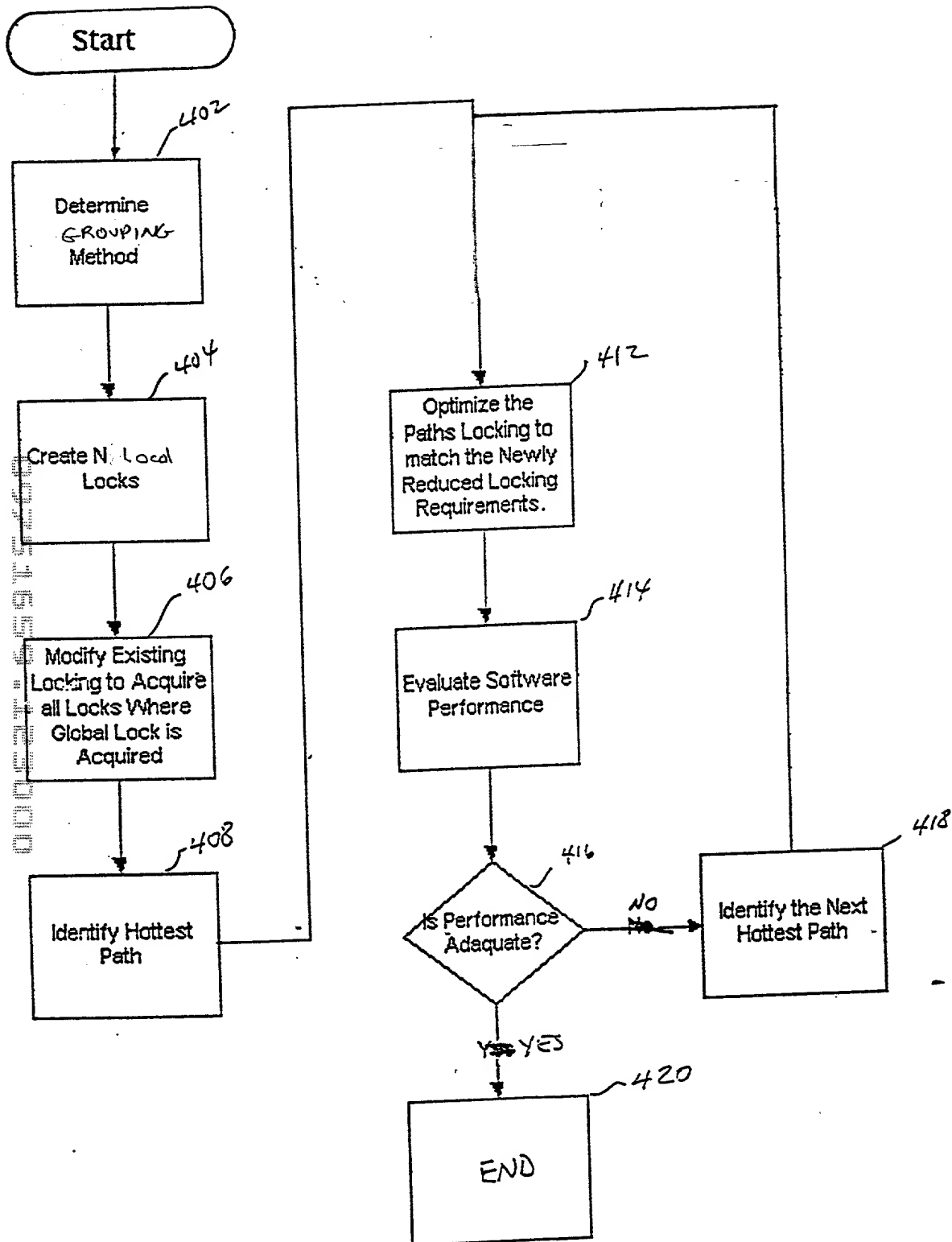


FIG. 7

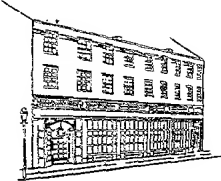


FIG. 8A

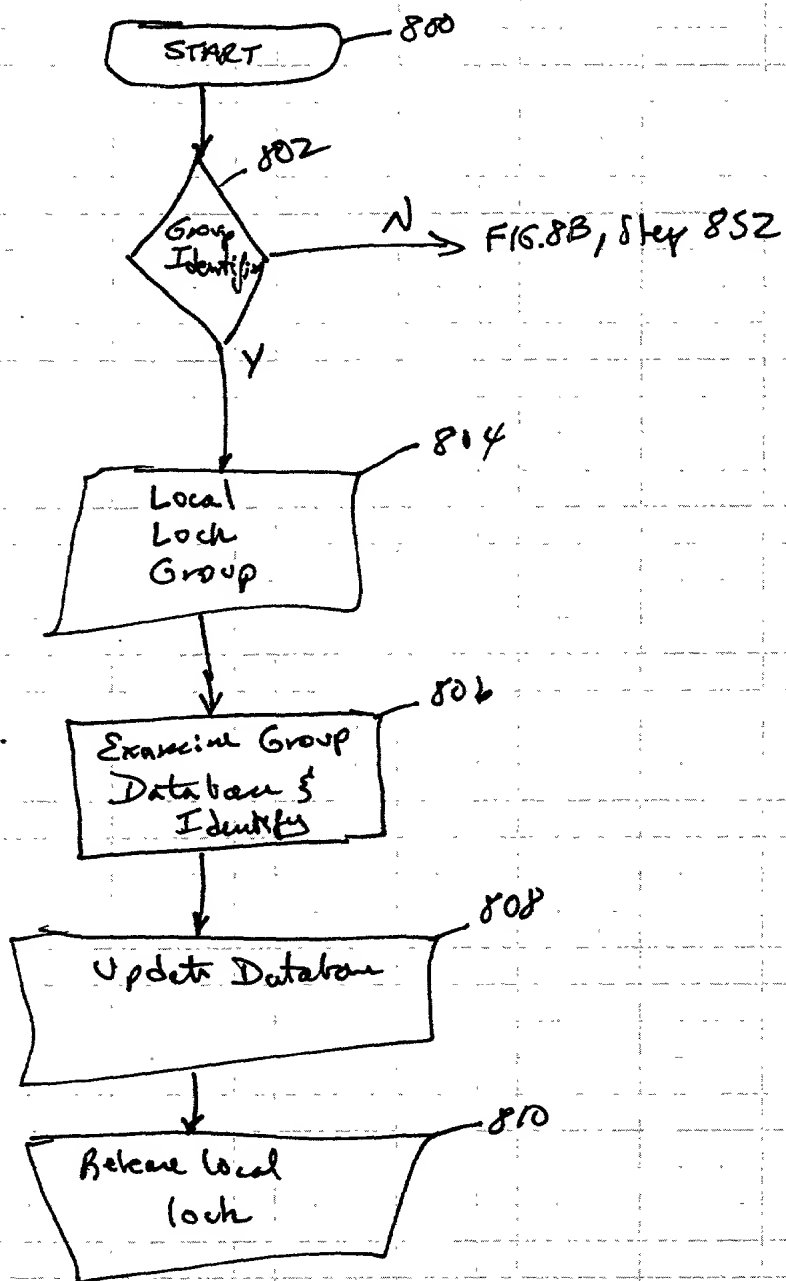


FIG. 8A





FIG. 8B

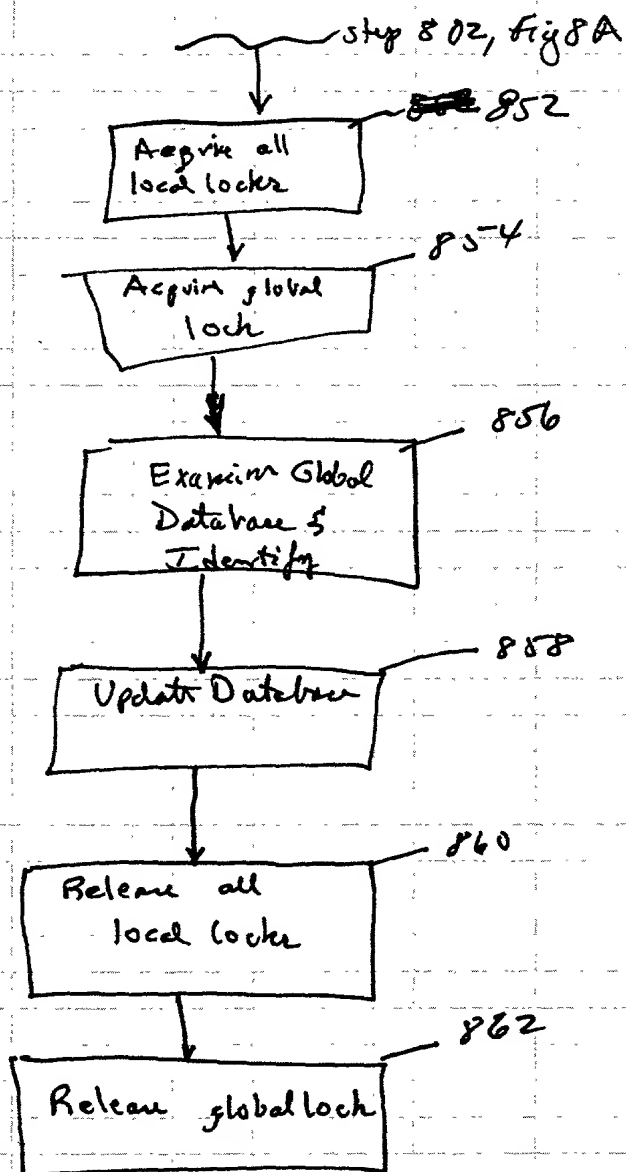


FIG. 8B